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Applicant Initiated Interview Request Form

Attorney Docket No.: P-3945-US

Application No.: 09/976,284 First Named Applicant: LOUZOUN, Eliel

Examiner: MASON, Donna K. Art Unit: 2111 Status of Application: Pending

Tentative Participants:

(1) **Naim Shichrur, Registration number 56,248** (2) **Dekel Shiloh**

(3) (4)

Proposed Date of Interview: **February 16, February 17 or February 21** **Proposed Time:** **9:30 or 10:00 AM** **(AM / PM)**

(1) ☒ **Telephonic** (2) ☐ **Personal** (3) ☐ **Video Conference**

Exhibit To Be Shown or Demonstrated: ☐ **Yes** ☒ **No**

If yes, provide brief description:

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims / Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) Rejection	claims 2, 4-6, 26, 27, 36-38, 40, 41, 56, 58, 59-62	US Patent 4428044 to Liron	☐	☐	☐
(2)			☐	☐	☐
(3)			☐	☐	☐
(4)			☐	☐	☐

☐ Continuation Sheet Attached

Brief Description of Arguments to be Presented:

Applicant traverses the rejection of claims 2, 4-5, 26, 27, 36-38, 40, 41, 56, 58-59, 61-62 in view of USPN 4428044, under U.S.C §102 , as well as the rejection of claims 6 and 60 under U.S.C §103(a). Attached is a proposed Amendment to the claims.

An interview was conducted on the above-identified application on _____

NOTE:
This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP §713.01).
This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

(Applicant/Applicant's Representative Signature) (Examiner/SPE Signature)

PROPOSED AMENDMENT (FOR DISCUSSION PURPOSES ONLY)

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. **(Cancelled)**

2. **(Currently amended)** A chip comprising:

at least two processing units with separate memories and separate busses, wherein said at least two processing units exchange data therebetween by transferring said data between said memories;

~~at least one~~ a first in first out (FIFO) unit to transfer said data between said busses;

~~at least one~~ a first direct memory access (DMA) channel to transfer said data from a first memory ~~one~~ of said memories to said ~~at least one~~ FIFO unit; and

~~at least one~~ a second DMA channel to transfer said data from said ~~at least one~~ FIFO unit to ~~another~~ a second memory of said memories,

wherein said data is transferred between said first and second memories via said first DMA channel, said FIFO unit, and said second DMA channel.

3. **(Canceled)**

4. **(Previously presented)** A chip according to claim 2 wherein said processing units are central processing units (CPUs).

5. **(Previously presented)** A chip according to claim 2 and further comprising at least two asynchronous clocks to control said at least two processing units.

6. **(Previously presented)** A chip according to claim 2 wherein one of said processing units is to process media access control (MAC) commands and another of said processing units is to process physical layer device (PHY) commands of a networking protocol.

7-25. (**Cancelled**)

26. (**Previously presented**) A chip according to claim 2 wherein said memories are random access memories (RAMs).

27. (**Previously presented**) A chip according to claim 2 and further comprising a common register accessible by said processing units to act as a channel of communication by which said processing units are to coordinate exchange of said data between them.

28-35. (**Cancelled**)

36. (**Currently amended**) A method for transferring data between processing units comprising:

sending data from a first processing unit embedded on a chip to a second processing unit embedded on said chip by establishing a first direct memory access (DMA) channel to a first in first out (FIFO) unit from a first memory directly accessible only by said first processing unit, and a second DMA channel from said FIFO unit to a second memory directly accessible only by said second processing unit, wherein said data is transferred between said first and second memories via said first DMA channel, said FIFO unit, and said second DMA channel.

37. (**Previously presented**) A method according to claim 36, wherein operation of said first DMA channel comprises any of the actions selected from the group consisting of:

transferring data from said first memory to said FIFO unit on request by said first processing unit;

waiting until said FIFO unit is not full before transferring each row of said data; and

notifying said first processing unit when all of said data has been transferred to said FIFO unit.

38. **(Previously presented)** A method according to claim 36, wherein operation of said second DMA channel comprises any of the actions selected from the group consisting of:

transferring data from said FIFO to said second memory on request by said second processing unit;

waiting until said FIFO unit is not empty before transferring each row of said data; and

notifying said second processing unit when all of said data has been transferred to said second memory.

39. **(Cancelled)**

40. **(Previously presented)** A method according to claim 36 wherein said first processing unit and said second processing unit are CPUs.

41. **(Previously presented)** A method according to claim 36 wherein said first memory and said second memory are RAMs.

42-55. **(Cancelled)**

56. **(Currently amended)** A device including a chip wherein said chip comprises:

at least two processing units with separate memories and separate busses, wherein said at least two processing units exchange data therebetween by transferring said data between said memories;

~~at least one~~ a first in first out (FIFO) unit to transfer said data between said busses;

~~at least one~~ a first direct memory access (DMA) channel to transfer said data from ~~one~~ a first memory of said memories to said ~~at least one~~ FIFO unit; and

~~at least one~~ a second DMA channel to transfer said data from said ~~at least one~~ FIFO unit to ~~another~~ a second memory of said memories.

wherein said data is transferred between said first and second memories via said first DMA channel, said FIFO unit, and said second DMA channel.

57. **(Canceled)**

58. **(Previously presented)** A device according to claim 56 wherein said processing units are central processing units (CPUs).

59. **(Previously presented)** A device according to claim 56 wherein said chip further comprises at least two asynchronous clocks to control said at least two processing units.

60. **(Previously presented)** A device according to claim 56 wherein one of said processing units is to process media access control (MAC) commands and another of said processing units is to process physical layer device (PHY) commands of a networking protocol.

61. **(Previously presented)** A device according to claim 56 wherein said memories are random access memories (RAMs).

62. **(Previously presented)** A device according to claim 56 wherein said chip further comprises a common register accessible by said processing units to act as a channel of communication by which said processing units are to coordinate exchange of said data therebetween.

63. **(Canceled)**.